I Claim:

1. A method for driving one-time operable isolation elements of a semiconductor chip, which comprises the steps of:

storing an item of isolation information in the semiconductor chip for each of the isolation elements to be operated on; and

beginning a one-time operation on a respective isolation element upon reception of the item of isolation information for the respective isolation element.

2. A method for driving one-time operable isolation elements of semiconductor chips, which comprises the steps of:

storing an item of isolation information in the semiconductor chips for each of the isolation elements to be operated on; and

beginning a one-time operation on a respective isolation element upon reception of the item of isolation information for the respective isolation element.

3. The method according to claim 2, which further comprises:

storing a first item of isolation information specific to each of the semiconductor chips beginning in an initial

semiconductor chip and then successively to further semiconductor chips and then to a last semiconductor chip for a first isolation element; and

storing a second item of isolation information for a second isolation element in the first semiconductor chip and continuing the storing of the second item of isolation information until the second item of isolation information has been stored in all the semiconductor chips after the last semiconductor chip receives the first item of isolation information.

4. The method according to claim 2, which further comprises storing the item of isolation information specific to each of the semiconductor chips in parallel for all of the semiconductor chips.

5. The method according to claim 3, which further comprises transmitting the first and second items of isolation information from a test device to the semiconductor chips through an interface.

6. The method according to claim 4, which further comprises transmitting the item of isolation information from a test device to the semiconductor chips through an interface.

7. The method according to claim 3, which further comprises effecting storage of the first and second items of isolation information such that the first and second items of isolation information are generated on a semiconductor chip itself.

8. The method according to claim 4, which further comprises effecting storage of the item of isolation information such that the item of isolation information is generated on a semiconductor chip itself.

9. The method according to claim 2, which further comprises forming the semiconductor chips integrally on a wafer.

10. The method according to claim 2, which further comprises disposing the semiconductor chips in a housed component.

11. A circuit configuration for operating on an isolation element, comprising:

an interface;

a first control line connected to the isolation element;

a buffer memory connected to said interface and receiving an item of isolation information through said interface, the item

of isolation information relating to the isolation element to be operated on; and

an isolation element driver connected to said buffer memory and to said first control line, said isolation element driver reading the item of isolation information from said buffer memory and effecting a one-time operation on the isolation element through said first control line upon a presence of the item of isolation information for the isolation element being stored in said buffer memory.